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Working Towards a Normally Off GaN Based MOSHEMT

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Working Towards a Normally Off GaN Based MOSHEMT

by

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Abstract

As the demand for smaller and more efficient electronics continues to grow, the technological advances of silicon begins to plateau. For this reason, researchers have been increasingly interested in other semiconductor materials, such as III-V semiconductors. Gallium nitride has proved to be a particularly useful material and research has gone into development of GaN based transistors, specifically the high electron mobility transistor (HEMT). One of the difficulties of the GaN based HEMT is creating a normally off device, while also limiting gate leakage. This thesis explores design possibilities for a MOSHEMT structure in an attempt to shift the threshold voltage as positively as possible. Specifically, options for the top semiconductor layer are explored and it is shown through TCAD simulations that due to lower spontaneous polarization, AlGaN is optimal for a less negative/more positive threshold voltage. Following this, options for the gate oxide are explored, including the use of multiple oxides. It is shown again through TCAD simulations that due to an electric dipole at the interface between high-k oxides and SiO_2, it is possible to create devices with thresholds shifted closer to a normally off device than with the use of a single gate oxide. All TCAD results are supported by a mathematical MOSHEMT model, and future directions for exploring the possibility of a normally off GaN based MOSHEMT are proposed.

1 Introduction and Motivation

1.1 Introduction to GaN

From the beginning of commercialized semiconductor devices, Silicon has been the industry leader and standard. Silicon has been the most researched, cheapest, and in many ways simplest semiconductor to work with. However, as Silicon begins to reach a plateau in terms of possible advancements, research interest has shifted towards the use and fabrication of different semiconductor materials. While Germanium is the only other elemental semiconductor, compound semiconductors can be created by combining two or more non-semiconductor elements, typically combinations of Group III and Group V elements.

Of these III-V semiconductors, Gallium Nitride (GaN) has proven a particularly useful material. Unlike Silicon, GaN is a direct bandgap semiconductor, meaning the maximum energy of the valance band and the minimum energy of the conduction band (where free holes and electrons are most likely to be found) are aligned with each other in terms of momentum vectors. This allows holes and electrons to be generated and recombined more efficiently, leading to overall higher device efficiency especially with regards to light absorbing/emitting devices such as solar cells and LEDs. The use of GaN and other III-V semiconductors have been the source of incredible innovations such as white LED light bulbs, offering

efficiencies significantly higher than previous incandescent or fluorescent bulbs. GaN also exhibits various other differences from Si, such as the fact that it is a polar material, naturally forms in a hexagonal wurtzite crystal structure, has a wide bandgap, and a high operating temperature. These properties make it a particularly interesting and promising material for use in other areas, such as transistors and power electronics.

1.2 Motivation for GaN Transistors

The trend in consumer electronics such as cell phones, computers, tablets, etc. over the years has been defined predominantly by one word: smaller. Consumers have continued to demand smaller electronics with more functionality. This has required engineers to fit increasingly more transistors on integrated circuits, and continually decrease the size of individual transistors. As transistor technology and fabrication techniques have improved, Silicon has been able to keep up with this demand. Unfortunately, as Silicon transistors reduce in size, the amount of leakage currents and therefore static power consumption drastically increases, as illustrated in Figure 1. Static power, which used to be relatively small and could be more or less ignored, has now surpassed dynamic power in terms of overall consumption by a significant factor. Increased static power consumption is of

course problematic for overall efficiency of electronics, resulting in limitations in battery life and size, two aspects which are very important to consumers.

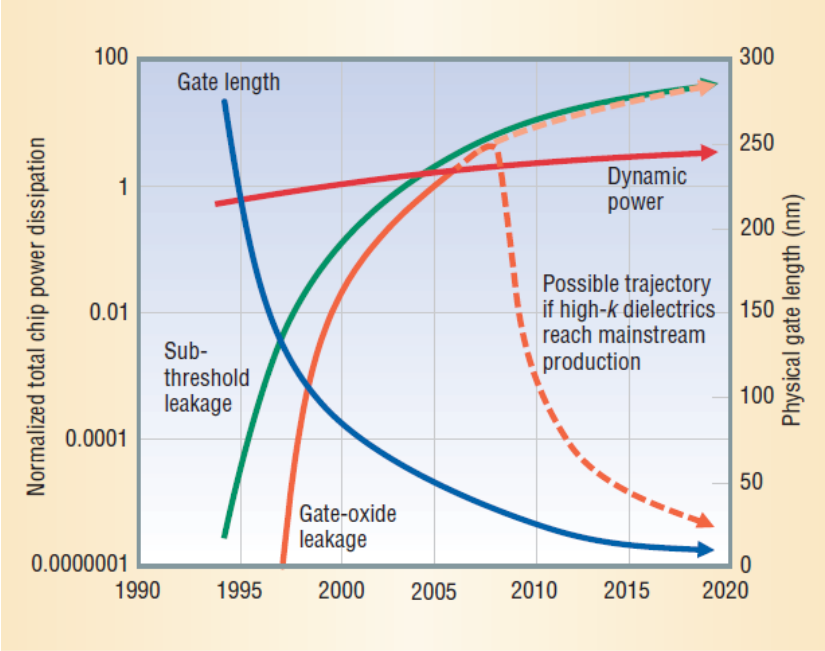

Figure 1: Silicon Transistor Size and Power Consumption [1]

In order to continue to decrease the size of electronics, while still offering higher efficiency/long battery life, other semiconductor materials must be considered as Silicon reaches its limit. As stated previously, Gallium Nitride, as well as other III-Nitride materials, have a wider bandgap and can offer less leaky transistors. Gallium Nitride also offers the possibility of lower on-resistances, further decreasing overall power consumption. It is for these reasons that research has begun in recent years on creating high efficiency GaN based transistors.

Typical integrated circuits predominantly utilize CMOS technology, relying on field-effect transistors (FETs). It is therefore desirable to create an analogous field-effect device when considering GaN based transistors. One example of this which a great deal of research has gone into is the High Electron Mobility Transistor (HEMT). This type of transistor relies on a two dimensional electron gas (2DEG) at the heterojunction between two different bandgap materials to conduct current between the source and drain. Similar to a MOSFET, a gate voltage applied to a HEMT is used to control the conductivity of this 2DEG. These types of transistors were first introduced in 1980, and have typically been made from other semiconductor materials such as InGaAs/GaAs. In recent years however research has been done on GaN based HEMTs, specifically AlGaN/GaN heterostructures.

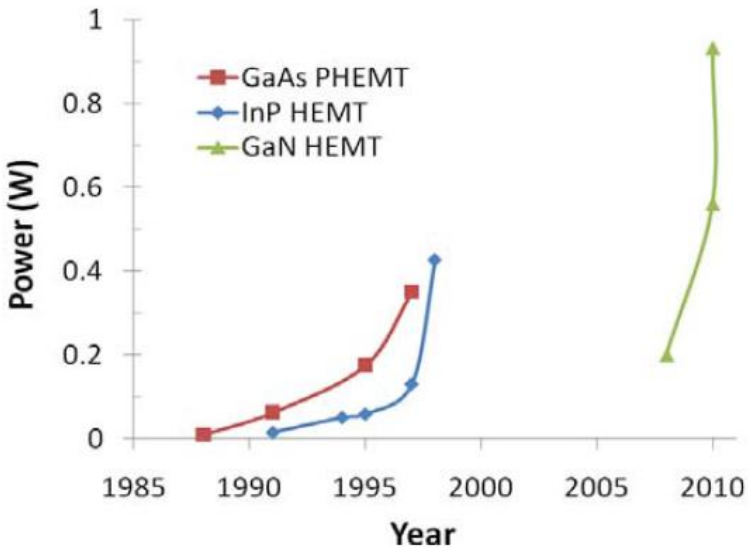

Figure 2: Power Outputs Demonstrated in HEMT Structures (94-95 GHz) [2]

The increasing attraction towards this material is due to its wide bandgap, high electron saturation velocity, and high electron concentration produced at the interface each leading to potentially high breakdown voltages, high frequency switch applications, and low on resistances [2]. Figure 2 shows that only 2 years after their commercial introduction, GaN based HEMTs had already far surpassed other materials in demonstrated power capabilities. One of the difficulties that has arisen with this technology which will be further discussed is creating a transistor which is “normally off”, also known as an enhancement mode transistor, with low leakages. This type of transistor would mean that if a bias of 0V is applied to the gate, the source and drain would not conduct any current and the transistor would have a positive threshold voltage. This thesis therefore discusses previous work on HEMT’s as well as explores potential options for the heterojunction and a 2 dielectric gate stack and layer to shift the threshold in a positive direction.

2 Background and Previous Work on GaN HEMTs

2.1 HEMT Structure

The main feature of the HEMT is the 2DEG formed at the interface between two semiconductor materials of differing bandgaps, specifically a wider bandgap material grown on top of a narrower bandgap material. Group III-V

semiconductors are obviously formed by 2 or more different elements, leading to a polarized crystal structure, and polarization-induced charge at material interfaces. The combination of spontaneous and piezoelectric polarizations creates a spike in the conduction band energy at this interface, dipping below the Fermi level. This spike is shown in Figure 3, which is taken from one of the TCAD simulations discussed later, showing both the conduction band energy as well as the Fermi level for an AlGaN/GaN interface.

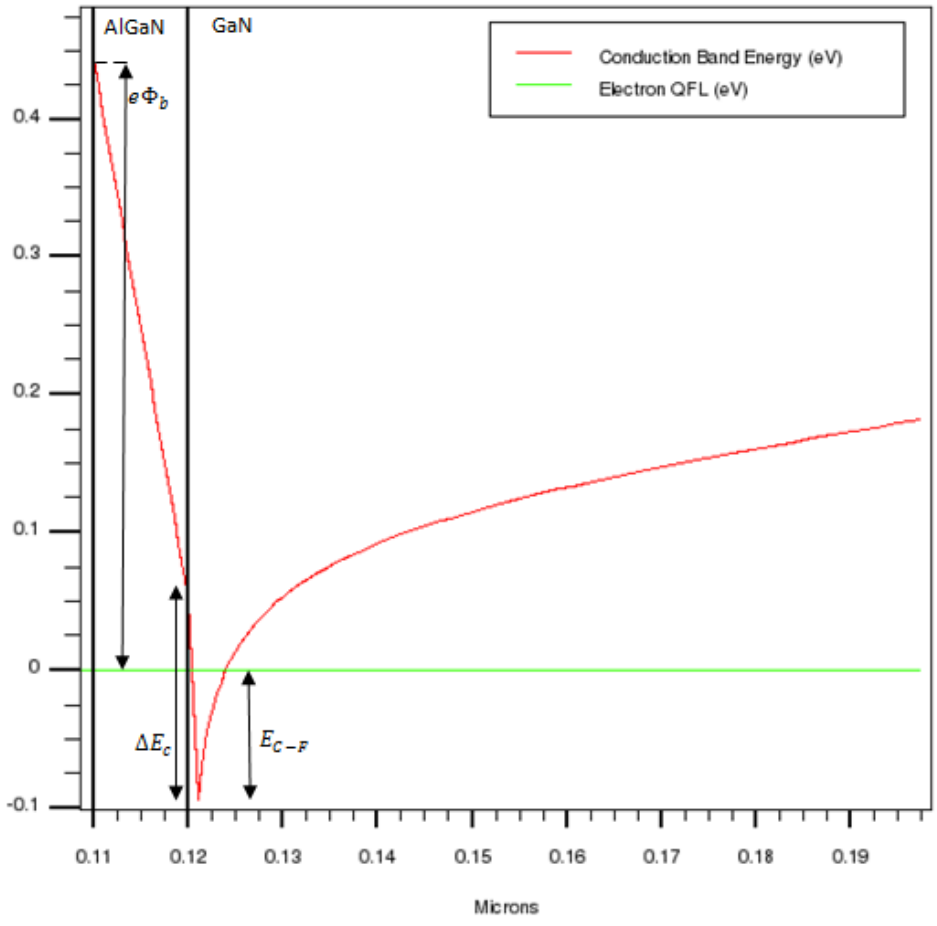

Figure 3: Conduction Band and Fermi Energy at an AlGaN/GaN Interface

This spike in the energy band resulting from the polarization charge creates a triangular quantum well near the interface in which a 2DEG is confined [3]. This well for a simple AlGaN/GaN interface is modeled in [3] and shown to have 2 predominant quantized energy states, E_0 and E_1, calculated using Schrödinger's equation and related to the 2DEG electron density, n_s, as follows:

$$E_0 = 2.123 * 10^{-12}(n_s^{2/3})$$

$$E_1 = 3.734 * 10^{-12}(n_s^{2/3})$$

The interface fixed polarization charge, σ, and sheet electron density of the 2DEG, n_s, as functions of the aluminum mole fraction, *x*, at an AlGaN/GaN interface are given in [4] by:

$$\sigma = P_{Tot}(GaN) - P_{Tot}(Al_xGa_{1-x}N)$$

$$n_s(x) = \frac{\sigma}{e} - \left(\frac{\varepsilon_0 \varepsilon(x)}{d_{AlGaN} e^2}\right)[e\Phi_b(x) + E_{C-F}(x) - \Delta E_c(x)]$$

where P_{Tot} is the total polarization (sum of spontaneous and piezoelectric polarizations), $\varepsilon(x)$ is the relative permittivity of the $Al_xGa_{1-x}N$ layer, $d_{AlGaN}$is the AlGaN layer thickness, $e\Phi_b$ is the Schottky barrier height at the gate/AlGaN interface, $E_{C-F}(x)$ is the penetration of the conduction band below the Fermi level, and $\Delta E_c(x)$ is the AlGaN/GaN interface conduction band offset. The different energy values are shown in Figure 3. This model could of course be

adapted for the interface between essentially any two III-V semiconductor materials.

A positive voltage applied to the gate metal above the AlGaN layer would attract more electrons to the interface, effectively increasing the conductivity of the 2DEG layer. This is analogous to the operation of the gate of a MOSFET affecting the inversion layer. In original HEMT structures, gate leakage currents were controlled and reduced by the Schottky barrier between the metal contact and semiconductor [4,5]. It was found that an additional GaN layer on top of the AlGaN/GaN structure would increase this Schottky barrier and therefore reduce the gate leakage [6]. Source and drain contacts on either side of the gate would then complete the HEMT structure, of which simplified cross sections are shown in Figure 4.

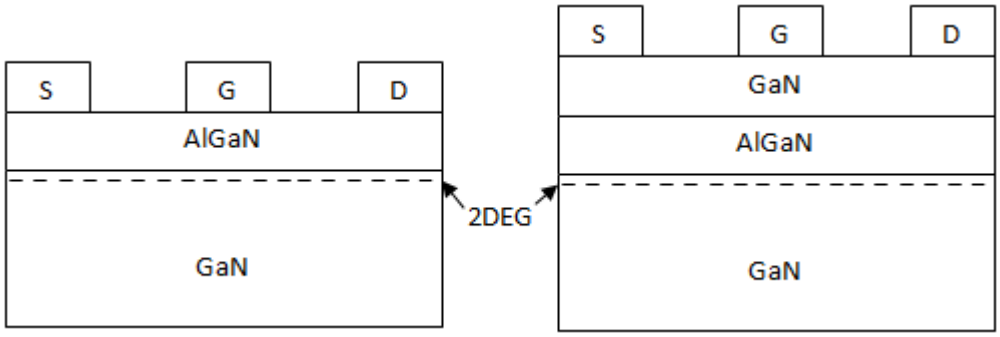

Figure 4: Simplified AlGaN/GaN Structure Without (Left) and With (Right) an Additional GaN Cap Layer

2.2 HEMT Gate Oxides – The MOSHEMT

As mentioned previously, HEMT gates consisted of a Schottky barrier which is what controlled the amount of gate leakage. As it turned out, this barrier was not extremely effective at suppressing gate leakage, especially as devices are scaled down. Therefore in recent years, research has gone into adding an additional insulating layer between the metal gate contact and semiconductor layers. In most cases, the insulators used are oxides, creating a metal-oxide-semiconductor HEMT (MOSHEMT) structure. Unlike Si MOSFETs in which a SiO_2 layer can created through thermal oxidation easily enough, thermal oxidation of Ga to create Ga_2O_3 is very slow for lower temperatures and high temperatures are likely to cause surface damage [7]. Oxide layers are therefore created on GaN based HEMTs through atomic layer deposition (ALD). While this requires a slightly more complex fabrication step, it allows for more options and control over the oxide layer chosen. Al_2O_3 is a frequently chosen oxide used in MOSHEMT devices due to its large bandgap, high breakdown field, high chemical and thermal stability, and ease of deposition [7, 8], although others have been and continue to be explored.

While the MOSHEMT structure is very effective at reducing gate leakage of the device as compared to a HEMT without an oxide layer, it is also accompanied by the undesired effect of a negative shift in the threshold voltage [8-18], which is typically already negative due to the presence of the polarization induced 2DEG at

a 0V bias. This negative shift is due to additional positive charge at the interface between the oxide and top semiconductor layer. The exact origin of this interface charge is not entirely understood and is seen with different oxide/semiconductor interfaces, but there are theories to help explain it. One theory on a contribution to this charge is the natural polarization of III-V materials inducting charge at the interface, similar to the contribution it makes to the 2DEG. However, a study [15] has shown that regardless of whether GaN is grown with a Ga top face or a N top face, the polarity of the charge seen at the interface with an oxide layer does not change, it remains positive for both. This result suggests that the oxide/III-V semiconductor interface charge does not come from the inherent semiconductor polarization, or at most it makes a negligible contribution, since the polarization charge would be expected to be opposite for oppositely grown semiconductor faces.

Another theorized origin of the oxide/III-V semiconductor interface charge is due to unexpected bonds between the elements of the oxide and semiconductor layers, particularly bonds between the group III elements and oxygen atoms, and other defects. This theory is presented in both [8] and [13]. They present research on atomic layer deposited Al_2O_3 on AlN and GaN. In both cases, a positive charge is seen at the interface between Al_2O_3 and the III-Nitride layer which they attribute to additional Al-O and Ga-O bonds at the interface.

Such bonds would effectively result in oxygen atoms substituting nitrogen sites, acting as donor dopants. This would create a positive interface charge and is supported by previous work in which the polarity of N-face GaN was reversed when an AlO_x layer was added [16]. Support for general interfacial defects as the origin of oxide/III-V interface charge come from [14] and [15]. In these studies it was shown experimentally that post metallization annealing was effective at reducing the interface charge between these layers. This supports that defects contribute to the positive interface charge, however a significant charge on the order of 10^{12}-10^{13} was still seen, demonstrating that surface defects are likely not the only source of charge, as was already theorized.

The final model for the presence of the oxide/III-V interface charge is the presence of energy states at the interface between the oxide and semiconductor conduction bands [8,10,11,12,17,18]. For an interface with density of states D_{it}, there exists a charge neutral energy level E_{CNL}. Levels above the E_{CNL} are acceptor states, and those below are donor states. Energy states above the Fermi level, E_{F0}, are viewed as being void of electrons, while those below the Fermi level are viewed as occupied by electrons. Therefore, if E_{F0} is located below E_{CNL}, there exist donor states which are void of electrons and positively ionized. This is the case demonstrated in [10,11,12,18] and the charge at the interface of the oxide and III-V semiconductor, Q_{it}, could then be calculated as

$$Q_{it0} = D_{it}q(E_{CNL} - E_F)$$

$$Q_{it} = Q_{it0} + D_{it}qV_{gs}$$

where Q_{it0} is the charge at zero gate bias.

2.3 Mathematical MOSHEMT Model

There have been several models generated to represent the HEMT device, and the subsequent MOSHEMT. These models are typically derived from solving Poisson's equation to solve for parameters such as the 2DEG sheet charge concentration. However, in order to better understand how some physical parameters, especially those relating to the oxide layer (thickness, relative permittivity, interface charge, etc.), a different model was created in [12] based on an energy band approach. This approach essentially calculates the various changes in the conduction band energy going through the device from the metal gate contact down to the bottom III-V bulk semiconductor. The model presented in [12] uses an AlGaN/GaN MOSHEMT structure but could be used for virtually any III-V MOSHEMT since the band structure will be unchanged aside from the magnitude of the different variables. In order to generalize the model, in this discussion the oxide layer will be referred to with the subscript "ox", the top semiconductor layer will be referred to with the subscript "top", and the bottom bulk semiconductor will be referred to with the subscript "bott" (e.g. ε_{ox}, ε_{top}, and ε_{bott} would be the permittivity of the oxide, top semiconductor, and bottom

semiconductor respectively). Aside from the changes in subscripts and where otherwise noted, the following mathematical model comes from [12].

As discussed, the core principle of the HEMT's function is the 2DEG created at the interface of the top and bottom semiconductors as a result of a quantum well created in the downward "spike" in the conduction band energy. The entire conduction band for the cross section of the structure is shown below.

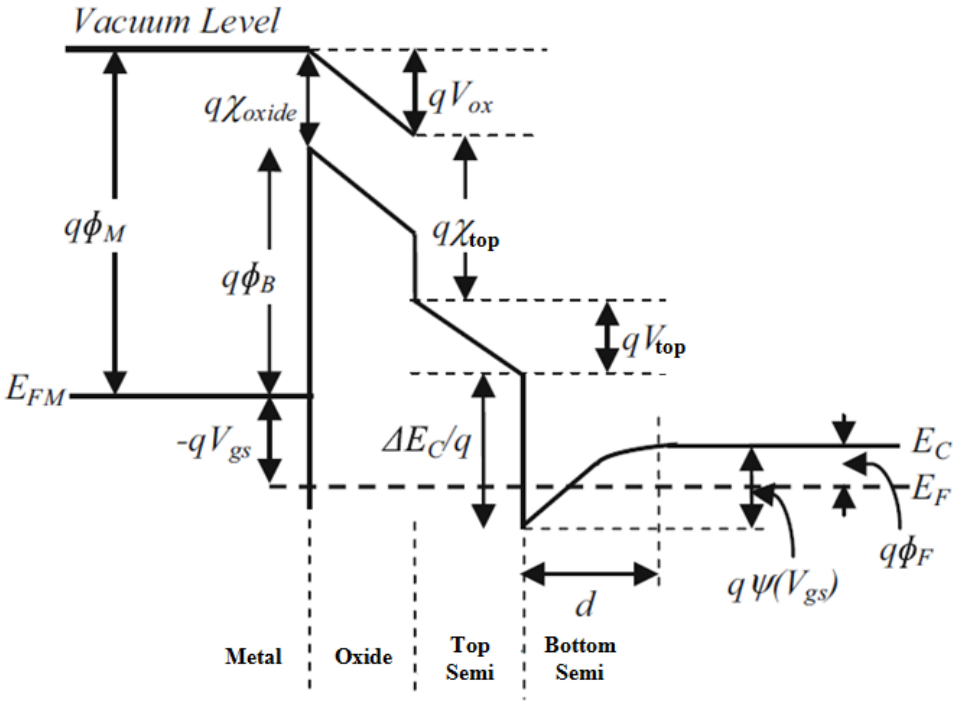

Figure 5: Typical HEMT Conduction Band [12]

The key quantity which will determine the functionality of the device is the surface potential at the surface of the bottom semiconductor at the interface with the top semiconductor layer, represented with $\psi(V_{gs})$ as it is a function of the gate

voltage. The larger this surface potential is, the larger the quantum well is which means a higher density and more conductive 2DEG. Conversely, when this surface potential drops to zero, the conductive channel of the 2DEG gets pinched off and no current can flow between the source and drain. The gate voltage at which this occurs is known as the flat band voltage (V_{FB}) and is very closely related to the operating threshold voltage of the device. While the threshold voltage and flat band voltage differ slightly, for the purpose of analyzing the effects of various physical parameters, the two voltages can be essentially viewed as the same since an increase or decrease in one corresponds to the same increase or decrease in the other. By simple addition and subtraction of the energy differences (taking note that the difference between E_{FM} and E_F is the negative of qV_{gs}), one can find two independent expressions for the total difference between the top of the vacuum energy level (E_{vac}) and the bottom of the quantum well conduction band (E_{min}),

$$E_{vac} - E_{min} = \phi_M - V_{gs} + \psi(V_{gs}) - \phi_F$$

$$E_{vac} - E_{min} = V_{ox} + \chi_{top} + V_{top} + \Delta Ec/q$$

These two expressions could then be set equal to one another and the surface potential solved for. Additionally, the work function of bottom bulk semiconductor, ϕ_s, is equal to $\chi_{top} + \Delta E_c/q + \phi_F$ and this can be subtracted from ϕ_M to give the difference between the metal and bulk semiconductor work

functions, a common and constant term when discussing these types of transistors, ϕ_{MS}. This gives an expression for the surface potential of,

$$\psi(V_{gs}) = V_{ox} + V_{top} - \phi_{MS} + V_{gs}$$

where V_{ox} and V_{top} are the voltage drop in the oxide and top semiconductor layers respectively, ϕ_{MS} is the metal-bulk semiconductor work function difference, and V_{gs} is the applied gate voltage.

In order to see the effects of the physical parameters of the oxide and top semiconductor layers, the voltage drops across them must then be expressed in terms of these parameters. The oxide layer can be modeled as a typical MOS capacitor, with capacitance

$$C_{ox} = \varepsilon_{ox}/t_{ox}$$

where ε_{ox} is the oxide layer's permittivity and t_{ox} is its thickness. The voltage across the oxide could then be modeled as with the voltage across any capacitor,

$$V_{ox} = \frac{Q}{C_{ox}} = \frac{Q_{ox} + Q_{it}}{C_{ox}} = \frac{t_{ox}(Q_{ox} + Q_{it})}{\varepsilon_{ox}}$$

where the charge is broken up into the charge spread in the oxide layer, Q_{ox}, and the interface charge between the oxide and top semiconductor, as discussed earlier and calculated with the interface energy state model. The voltage drop across the top semiconductor layer can be expressed in a similar way,

$$V_{top} = \frac{q * \sigma_{pol} * t_{top}}{\varepsilon_{top}}$$

where σ_{pol} is the sum of the spontaneous and piezoelectric polarization charges, t_{top} is the top semiconductor thickness, and ε_{top} is the top semiconductor permittivity.

Combining the equations for the voltage drops in each layer, the equation for the surface potential, and the equation for the oxide/top semiconductor interface charge yields a final result for the surface potential in terms of physical parameters as,

$$\psi(V_{gs}) = \frac{t_{ox}(Q_{ox} + Q_{it0})}{\varepsilon_{ox}} + \frac{q * \sigma_{pol} * t_{top}}{\varepsilon_{top}} - \phi_{MS} + \left(1 + \frac{t_{ox}(q * D_{it})}{\varepsilon_{ox}}\right) V_{gs}$$

As stated earlier, the flat band voltage V_{FB} occurs as the surface potential goes to zero. This value can therefore be found by setting the left side of the equation equal to zero and solving for V_{gs}, yielding a flat band voltage of

$$V_{FB} = \frac{\left(\phi_{MS} - \frac{t_{ox}(Q_{ox} + Q_{it0})}{\varepsilon_{ox}} - \frac{q * \sigma_{pol} * t_{top}}{\varepsilon_{top}}\right)}{1 + \frac{t_{ox}(q * D_{it})}{\varepsilon_{ox}}}$$

This model shows how positive charges at the oxide/top semiconductor interface can further reduce the flat band voltage as suggested previously. If negative charge could be created in the oxide or at its interface, this would aid in counteracting the inherent positive interface charge and shift the flat band and threshold voltages in a positive direction, towards a normally off device [18].

3 Top Semiconductor Material Effect on Threshold Voltage

3.1 Choosing the Top Semiconductor Material

In trying to design and optimize a MOSHEMT, one of the obvious aspects that could be changed is the material used. This can apply to any of the layers, although perhaps the most important would be the top semiconductor layer, as the polarization due to the interface between this layer and the bulk semiconductor is predominately responsible for the formation of the 2DEG. This importance in the mathematical model is seen with the $\frac{q*\sigma_{pol}*t_{top}}{\varepsilon_{top}}$ term in the expressions for the surface potential and threshold voltage. The material chosen for the top semiconductor layer will determine the values of the total polarization charge at the interface, σ_{pol}, as well as the layer's permittivity, ε_{top}, and the layer's thickness could be adjusted.

In theory, one should be able to choose any semiconductor material for this top layer in order to tweak the performance of the device exactly as desired. In practice however, this is not the case. When creating a heterostructures between two different semiconductors, an important value which must be taken into account is the lattice constant of each. If the semiconductors have different lattice constants, there will be strain induced in the material. This strain is what is responsible for piezoelectric polarization at heterojunctions, but if the strain is too large, dislocations will occur [19]. Dislocations in a semiconductor may have

unwanted effects, such as reducing carrier mobility and overall device performance. Therefore, when choosing the material for the top semiconductor layer of a MOSHEMT, only materials with lattice constants relatively close to that of GaN can be used in practice. As shown in Figure 6 taken from Ref. [20], this limits the material options to essentially only AlGaN and AlInN. Compositions of $Al_{0.25}Ga_{0.75}N$ and $Al_{0.83}In_{0.17}N$ give lattice constants close enough to GaN to not cause dislocations, and so these composition fractions will be used and can be assumed for the remainder of this thesis.

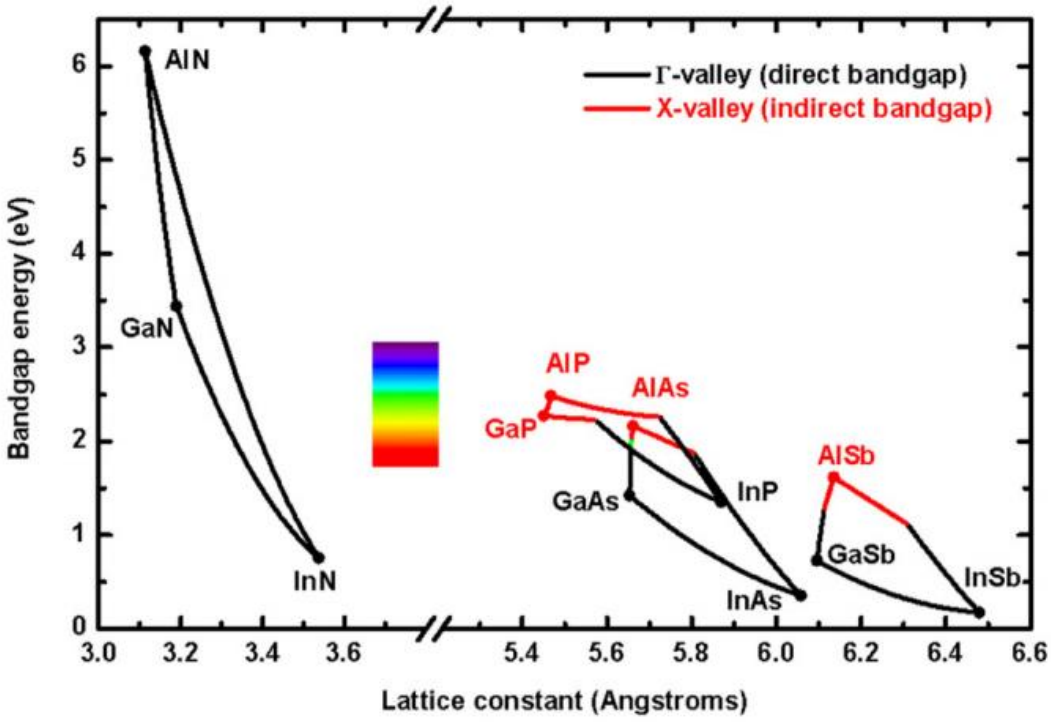

Figure 6: III-V Semiconductor Lattice Constants and Bandgap Energy [20]

As mentioned, the two parameters in the MOSHEMT mathematical model determined by the material chosen for the top semiconductor are the permittivity and the induced polarization charge. It has been shown that AlInN exhibits significantly higher spontaneous polarization, as compared to AlGaN, due to the much higher content of aluminum when lattice matched to GaN [10,21]. This would theoretically lead to a higher electron concentration in the 2DEG, which could be useful to allow high current densities [10] and high speed transistors [21]. This however may be a hindrance in trying to create a normally off device, as seen by the increase of the negative $\frac{q*\sigma_{pol}*t_{top}}{\varepsilon_{top}}$ term in the expression for the threshold voltage associated with an increase in σ_{pol}. In order to further investigate the effect of the top material choice on the device's threshold voltage, simulations were done using TCAD software and discussed in the following section.

3.2 Simulating the AlGaN/GaN versus AlInN/GaN HEMTs

In order to simulate the effects of choosing different materials for the top semiconductor layer of the MOSHEMT, 2 dimensional models were made using the Atlas device simulator created by Silvaco. Along with the Blaze module, this software allows for accurate simulation of the physics of a large library of materials; including binary, ternary, and quaternary semiconductors as well as

various oxides. Using the deckbuild environment, a simple, typical MOSHEMT structure was created, an example of which can be seen in Figure 7. This structure consisted of a conductive gate electrode surrounded by a nitride insulator on top. Below this is an oxide layer; 10nm thick SiO_2 was chosen for these simulations although others can be used, the effects of which will be discussed in Chapter 4. The top semiconductor material is below the oxide, the thickness of which was varied from 20nm down to 1nm; and finally bulk GaN extends from the bottom of the top semiconductor layer down to 2um (not fully shown in Figure 7 due to zooming). Conductive source and drain contacts were created on either side of the gate contact, extending down into the GaN bulk where the 2DEG channel would be created. Finally to complete the structure design, a mesh was created to simulate, with the largest amount of nodes/smallest spacing seen of course near the oxide and top semiconductor layers and where the 2DEG would be created.

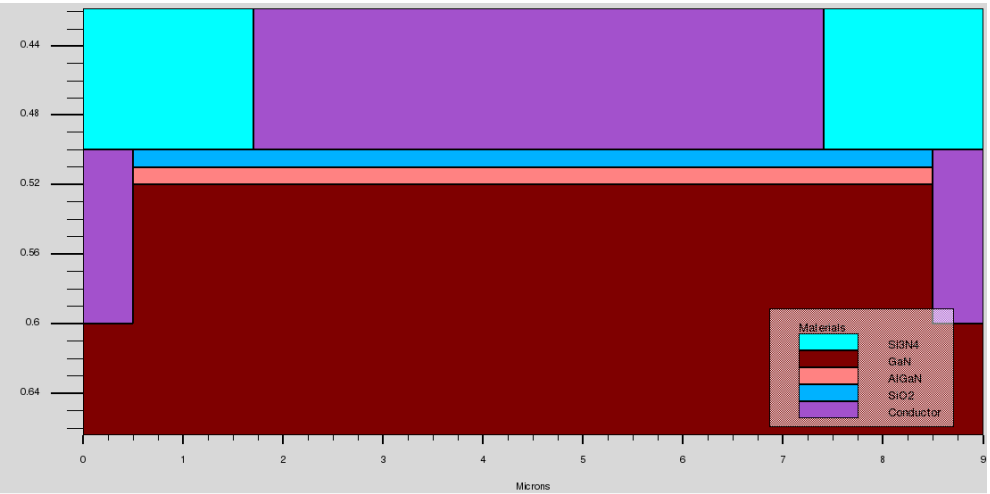

Figure 7: Example of Atlas MOSHEMT Structure for Simulation

The created structure was then simulated, ensuring calculation of the polarization charge due to both spontaneous and piezoelectric polarization, first for the condition of zero applied bias to any of the contacts. A cut line was made vertically in the center of the device to extract the conduction band energy and Fermi level, as shown in Figure 8. The conduction band energy matches that shown in Figure 5, used to create the mathematical model. This confirms the validity of both the mathematical model as well as the simulation. Furthermore, the conduction band energy spike below the Fermi level indicates the existence of a 2DEG with zero gate bias, meaning the normally on device.

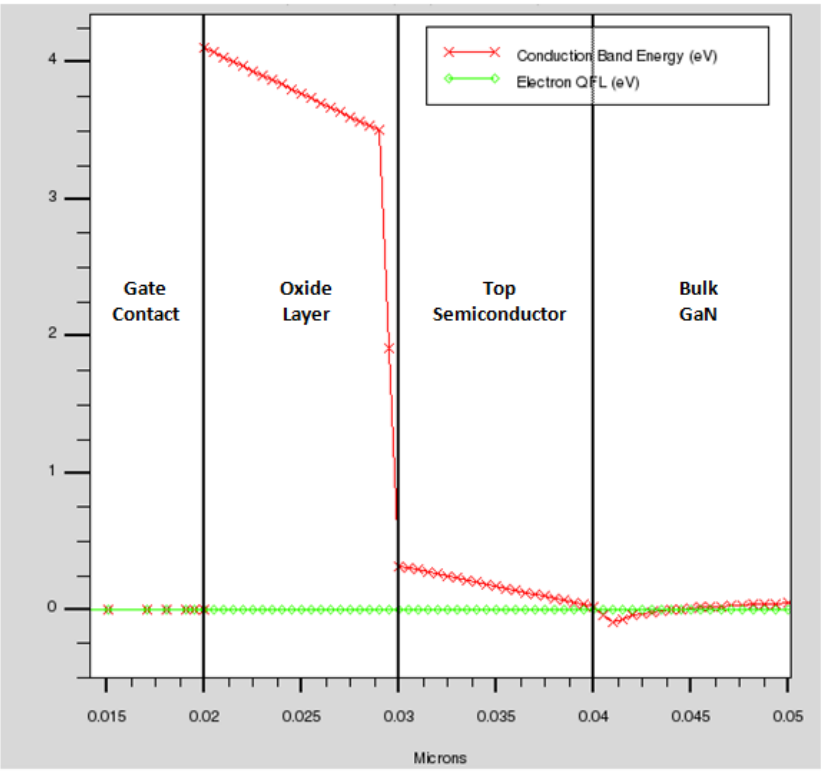

Figure 8: Simulated Conduction Band at Zero Bias

Once the simulation model was validated, the device could be simulated for different biases and the effects of changes to the top semiconductor layer could be viewed. The drain contact was biased at 1V for all simulations, and the gate voltage varied 0 zero to -20V in intervals of -0.05V, with Atlas solving for the DC solution at each bias point. The I_d-V_{gs} curve was then plotted using Tonyplot, an example of which is shown below in Figure 9 for an AlGaN/GaN structure with t_{AlGaN}=10nm.

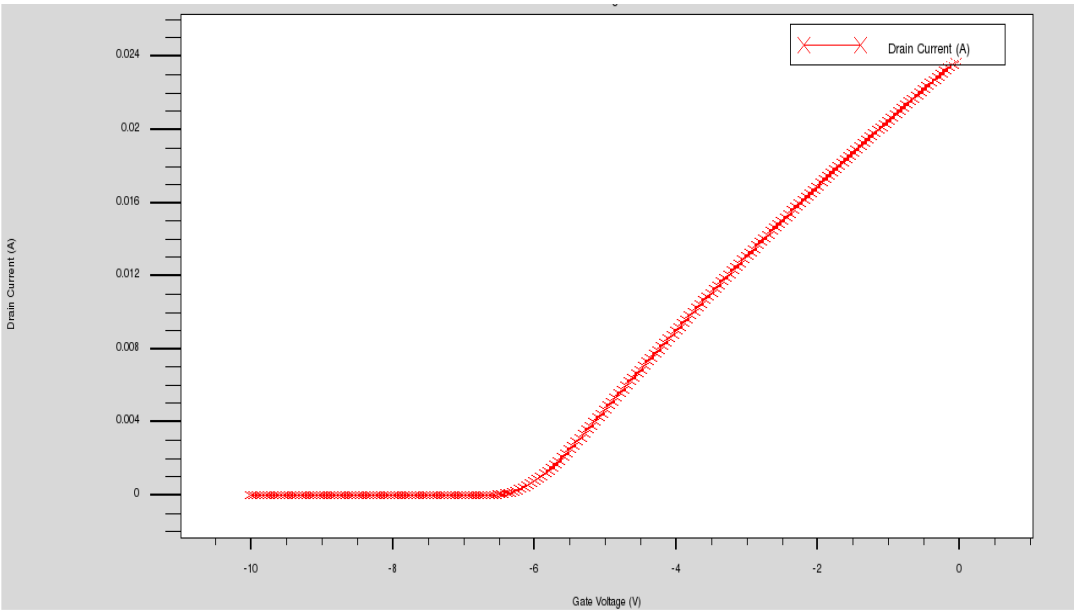

Figure 9: Typical Simulated MOSHEMT I_d-V_{gs} Curve

The curve of the drain current appeared as expected, showing a negative threshold value and therefore as stated, a normally on device. The effects of using an AlGaN layer versus an AlInN layer were then explored, simulating each as stated previously for thicknesses varying from 20nm to 1nm. The threshold

voltage was defined as the gate voltage at which the drain current is equal to 1mA for a drain bias of 1V, and was extracted for each of the simulations run. The results of the threshold voltage dependence on the top semiconductor material and thickness are shown below.

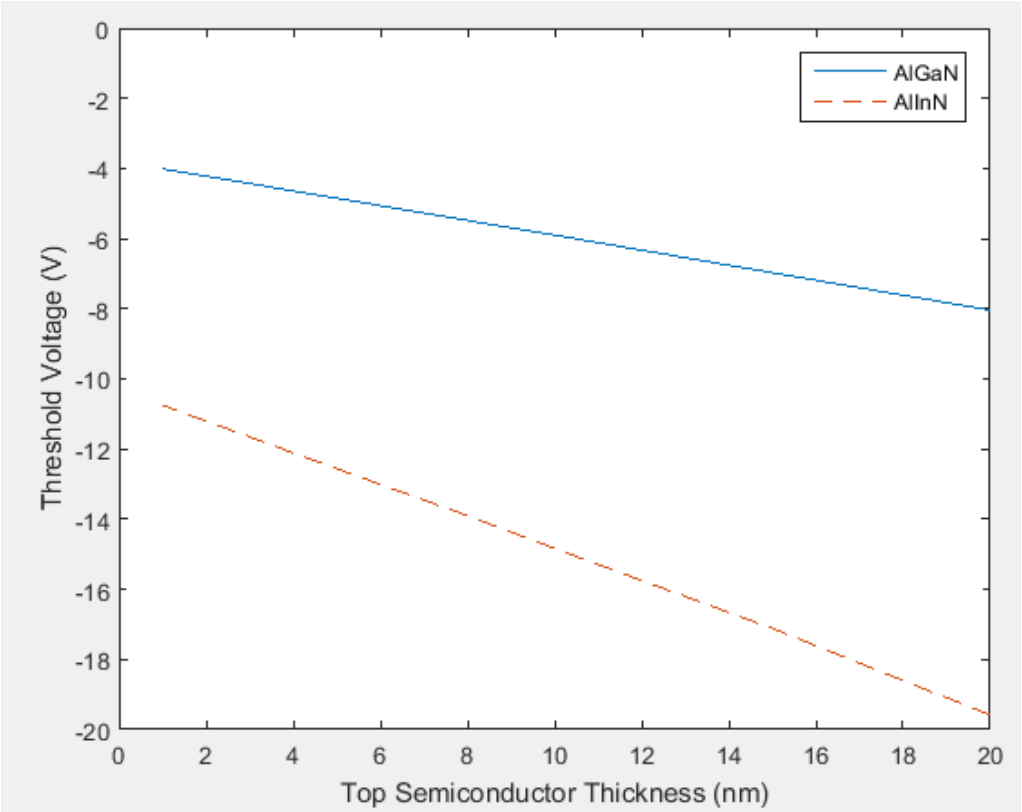

Figure 10: Threshold Voltage Dependence on Top Semiconductor Material and Thickness

The results of the simulation essentially confirm expected results. Looking back at the expression found for a MOSHEMT threshold voltage, the $-\frac{q*\sigma_{pol}*t_{top}}{\varepsilon_{top}}$ term indicates that there should be a negative, linear relation between the top

semiconductor thickness and the threshold voltage. This relation is seen in the simulation results and agrees with the results seen in literature [10,12,18]. Furthermore, it was expected that the higher aluminum content in AlInN would lead to a significantly higher spontaneous polarization charge [10,21], which would be expected to cause a more negative threshold voltage as compared to AlGaN. This expectation can also be seen and confirmed by the simulation results which show an AlInN/GaN threshold voltage about 7-12V lower than the AlGaN/GaN threshold voltage depending on thickness. While the AlInN/GaN device has been reported to potentially offer advantages such as high switching speeds and sheet carrier density [21]; it can be concluded that for the efforts of working towards a normally off device, an AlGaN top semiconductor layer seems to be the more desirable material.

4 Adjusting Threshold Voltage With High-K/SiO_2 Gate Stack

4.1 High-k/SiO_2 Interface Dipole

The other negative term in the expression for the MOSHEMT threshold voltage is the one relating to the oxide layer, $-\frac{t_{ox}(Q_{ox}+Q_{it0})}{\varepsilon_{ox}}$. Therefore it seems obvious that changes to the oxide layer could change the threshold voltage of the device, and potentially help in working towards a normally off device. Of course one change that could be made is the specific oxide used for the gate. Going a step

further however, it is also possible to use multiple different oxides layered in the gate. Typically, since the gate oxide is modeled as a capacitor, the use of multiple oxide layers would be modeled as multiple capacitors in series with one another with the capacitance of each determined by the individual oxides used. When the oxide stack consists of a high-k dielectric, such as Al_2O_3 or HfO_2, combined with SiO_2 however, an additional effect is seen. This additional effect is the formation of an electric dipole at the high-k/SiO_2 interface [22-25].

There have been several theories proposed to explain the existence of this electric dipole. One theory presented in [22] is based on the band line up and existence of dielectric contact induced gap states (DCIGS). This theory suggests the existence of energy states at the interface between the oxides, similar to the theory for the charge at the oxide/semiconductor interface. According to this theory, the charge neutral levels (CNL) of the two oxides are different before contact. When the oxides are joined, electrons are transferred either to or from the SiO_2 to equalize the CNL and Fermi level at either side of the interface. This transfer of electrons results in a voltage difference, or dipole, across the interface. The magnitude and direction of this dipole is therefore determined by the difference between the separate oxides' CNLs. While this model has been shown to match up with some experimental results [22], it is not sufficient to explain all

experimental results, such as why a dipole is not seen at a high-k/high-k interface [23,24].

A deeper theory for the origin of the high-k/SiO_2 dipole is given by [23] explaining its formation on a molecular level. This theory suggests that the dipole is a result of an areal density difference of oxygen atoms. When the high-k oxide and SiO_2 are brought together, the difference in oxygen atom densities results in a movement of oxygen atoms from the higher density to lower density material at the surface. This would result in negatively ionized oxygen in the material which had a lower areal density, and a net positive charge due to oxygen vacancies in the material which had a higher areal density. This would again mean a dipole at the interface, the magnitude and direction of which would depend on the areal density difference between the two. When the ratios of areal densities between SiO_2 and different high-k oxides are compared to experimental results of flat band voltage shifts in such structures, the results match up very well, strongly supporting this theory [23,24,25]. The lack of a dipole at high-k/high-k interfaces is also suggested by this theory. SiO_2 has highly covalent bonds, while high-k oxides tend to have much closer packed ionic metal-oxide bonds. The deformation of the SiO_2 covalent bonds would result in a much higher driving force for the migration of oxygen atoms than the ionic bonds in high-k oxides.

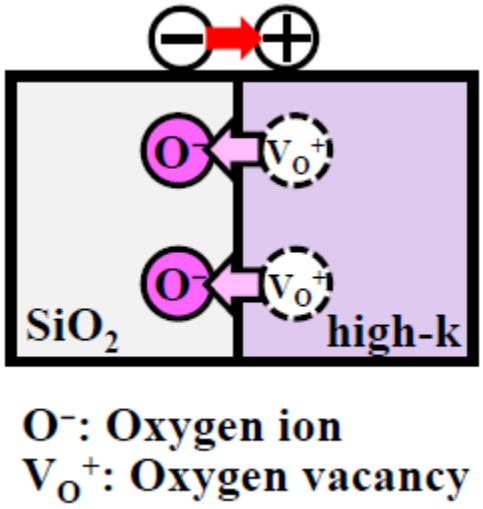

Figure 11: High-k/SiO_2 Interface Dipole Due to Oxygen Migration [24]

This theory was very recently further supported by [24] in which classical molecular dynamic simulations were performed for various high-k/SiO_2 interfaces. In these simulations, the migration of atoms was seen, and led to the formation of silicate layers at the interface. It was suggested that in high-k dielectrics with lower oxygen densities, the migration of metal ions to the SiO_2 layer may also be responsible for the dipole formed. Regardless of which atoms migrate however, this theory/model provides several important facts with regard to the effects it may have on a threshold voltage. The first of these is once again that no dipole is formed at the interface of two high-k oxides. A second is that the dipole formed and subsequent shift in threshold voltage is relatively independent of the thickness of the oxide layers, assuming they are at least thick enough for the formation of the interfacial silicate layer. Finally, the migration of atoms could be increased at higher temperatures [24], which means although it has not been

experimentally shown, the dipole induced threshold shift could be increased by thermal annealing.

4.2 High-k/SiO_2 Gate Stack Simulations

Similar to in chapter 3, the effects of different and multiple oxide layers were investigated through the use of simulations with the Atlas software. This study specifically investigated SiO_2, Al_2O_3, and HfO_2 since Al_2O_3 and HfO_2 are the only high-k dielectrics shown to induce a positive dipole induce threshold voltage shift when combined with SiO_2 [23,24]. Using the same general setup as in Chapter 3, simulations were first run for single oxide gates of varying thickness. AlGaN was chosen as the top semiconductor layer, as it was determined to be most desirable. Each of the oxides was varied in thickness from 10nm down to 0nm. The drain was again biased at 1V and the threshold voltage was defined as the gate voltage at which the drain current equaled 1mA. The results of this simulation are shown below.

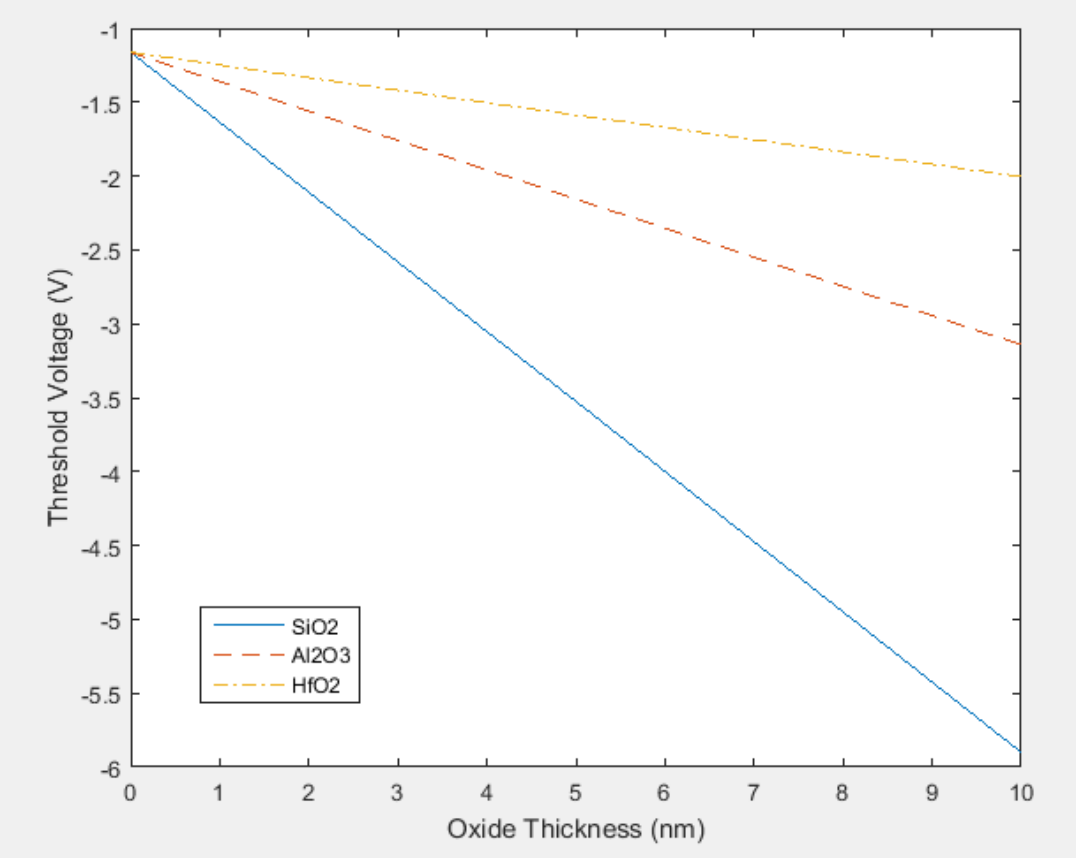

Figure 12: Threshold Voltage Dependence on Single Oxide Thickness

The results for the single oxide layer show a negative linear relation between threshold voltage and oxide thickness for each of the three oxide layers. SiO_2 shows the greatest negative shift with increasing thickness, while HfO_2 shows the least negative shift. These results match very well with the results seen in [11,14,18]. Furthermore, the results can be explained by the expression for threshold voltage derived in Chapter 2. This expression contains the term $-\frac{t_{ox}(Q_{ox}+Q_{it0})}{\varepsilon_{ox}}$. This clearly agrees that there should exist a negative linear relationship with oxide thickness. It also shows that oxides with a higher

permittivity should show less of a negative shift in threshold voltage than those with a smaller permittivity. Seeing as the relative permittivities of SiO_2, Al_2O_3, and HfO_2 are about 3.9, 9.1, and 25 respectively [26], the fact that SiO_2 shows the most negative shift and HfO_2 shows the least negative shift also agrees with the mathematical model. This information suggests that using an HfO_2 layer would be the best choice for attempting to create a normally off MOSHEMT device. However as discussed in the previous section, the use of a high-k/SiO_2 stack would create a dipole induced threshold voltage shift, which could prove to provide a threshold voltage even closer to a normally off device.

As mentioned earlier, the best theory for the formation of the high-k/SiO_2 interface dipole comes from the migration of oxygen (or metal) atoms to or from the SiO_2 layer [23,24]. This should create a dipole and subsequent threshold shift independent of layer thicknesses. Simulations were run for MOSHEMT structures with both an Al_2O_3/SiO_2 and an HfO_2/SiO_2 gate stack. The Al_2O_3/HfO_2 stack was not considered as no dipole is formed as such a high-k/high-k interface [23] and such a stack should therefore not be able to achieve a threshold any more closer to positive than either individual oxide.

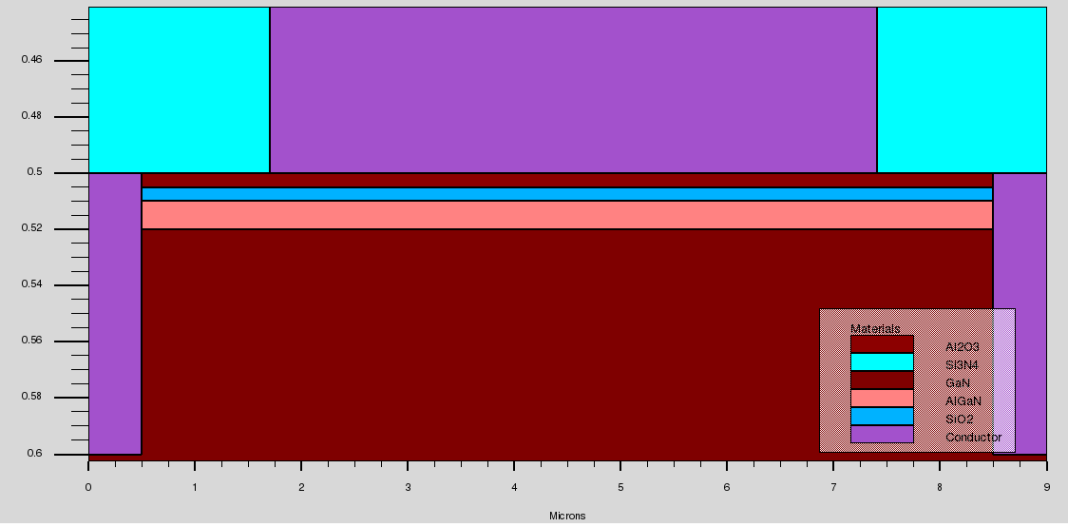

Figure 13: Example of MOSHEMT Structure with High-k/SiO_2 Stack for Simulation

The Al_2O_3/SiO_2 and HfO_2/SiO_2 interfaces were experimentally determined to generate dipole induced flat band voltage shifts of 0.55V and 0.3V respectively [25]. These shifts were modeled in the TCAD simulations as sheet charges corresponding to the same shift. The simulations were then run for various thicknesses of the oxides. In order to compare, the sum of the two oxides was kept at a constant 10nm. The thickness of the silicate layer found to be produced in [24] was found to be 0.27nm, and so this was assumed to be the minimum thickness of either oxide required to attain the same dipole and threshold shift. Therefore, the thickness of the high-k oxide in each was varied from 0.27-9.73nm, with the SiO_2 thickness equaling 10-$t_{high\text{-}k}$ nm. The results of these simulations are shown below and compared to the thresholds of the single oxide devices.

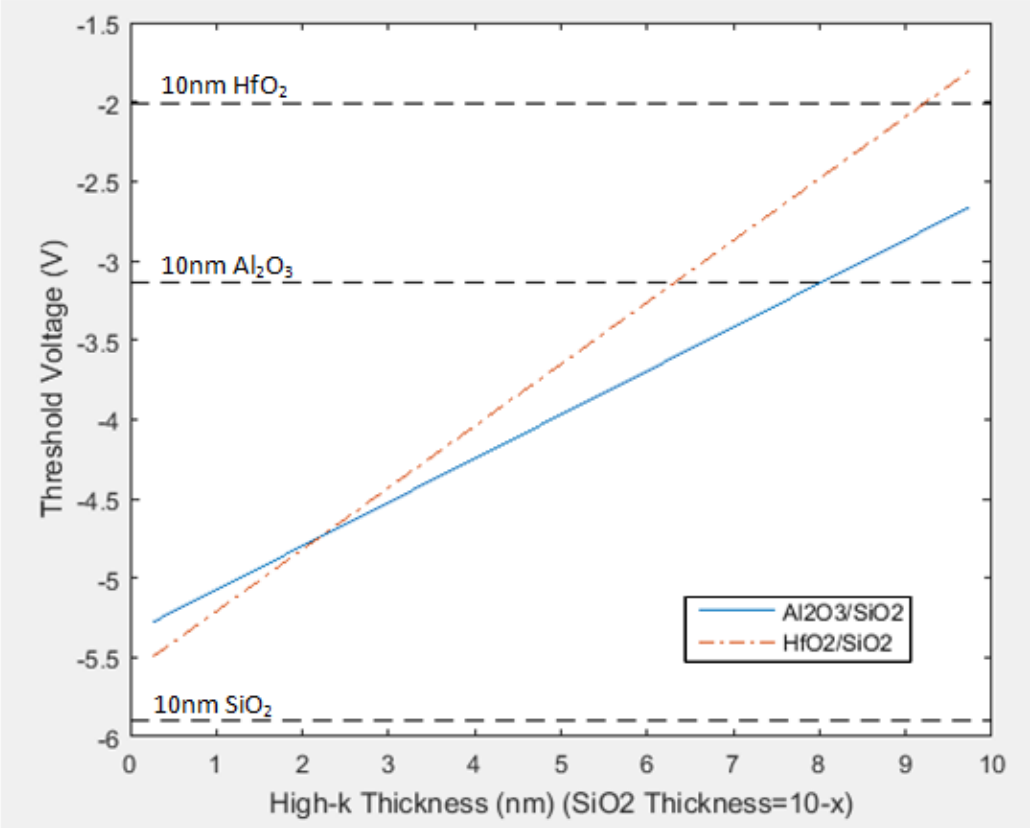

Figure 14: Threshold Voltage for High-k/SiO_2 Gate Stack

Although the Al_2O_3/SiO_2 interface had a larger dipole, it is seen that when the SiO_2 layer thickness is reduced, the HfO_2/SiO_2 gate stack can attain a less negative voltage, surpassing that of the HfO_2 single layer device of the same thickness. If total oxide thickness is further reduced, it seems logical that the threshold voltage would shift even more positively in comparison and may even be able to reach or surpass the threshold seen with no gate oxide. This is a very important finding, that it may be possible through the use of a high-k/SiO_2 stack to negate the

negative threshold shift seen as a result of adding an oxide layer, while still maintaining the leakage reduction of the oxide.

5 Conclusions and Future Directions

This thesis has discussed the physics and models related to gallium nitride based metal oxide semiconductor high electron mobility transistors. It then went on to explore the different design options for the top semiconductor layer as well as the oxide layer in an attempt to move towards a normally off device. With regards to the top semiconductor layer, it was shown that the use of AlInN shifts the threshold voltage negatively as compared to AlGaN, and therefore if a normally off device is desired then AlGaN would be the better material. In the study of oxide layers, three oxides were considered; SiO_2, Al_2O_3, and HfO_2 as well as the Al_2O_3/SiO_2 and HfO_2/SiO_2 stacks. For this it was found that HfO_2 provides the overall least negative threshold voltage, however it can be combined with a thin SiO_2 layer to further shift the threshold voltage in a positive direction. Other oxides could be explored, however high-k/high-k interfaces do not benefit from any dipole formation, and Al_2O_3 and HfO_2 are the only high-k oxides predicted to create a positive threshold shift based on the best theory for the interface dipole formation [23,24].

Moving forward, the results attainted from the mathematical model and simulations presented in this thesis should of course be confirmed experimentally. To this end, there are several factors that may affect the experimental device performance which are related to but outside the scope of this thesis. One of these factors is simply fabrication quality. Much of what was presented in this thesis is dependent on particular surface charges and interactions between layers of different materials. These can be greatly affected by things such as defects during fabrication which may degrade device performance. If however particular defects can be purposefully created, such as additional negative charge being presented in the oxide layer or at its interface, it is possible this will improve the device, as such defects would assist in positively shifting the threshold voltage. In general however, care must be taken during fabrication to avoid unwanted defects in what is likely to be a sensitive device.

Another area which could be explored in future work is the use of thermal annealing and its effects on device performance. It has been mentioned that other work has shown post metallization annealing to be beneficial in positively shifting the threshold voltage of HEMT devices by reducing the oxide/semiconductor interface charge [14,15]. Furthermore, it has been suggested that increased temperatures could increase the migration of atoms at a high-k/SiO_2 interface [24]

leading to dipoles of larger magnitude and greater shifts in threshold voltage, potentially assisting in the creation of a normally off device.

A final practical aspect that could be explored is the frequency response of the designs suggested in this work, particularly designs with multiple gate oxides. The frequency response of these devices will be particularly interesting due to the Maxwell-Wagner polarization effect. The Maxwell-Wagner instability model states that for a stack of two different dielectrics, the final state of the electric field in each when a given voltage is applied is not proportional to the dielectric constant of each, but rather is determined such that the current density through each is equal [27]. This means that charge must accumulate at the interface until this condition is met. This charge takes some time to accumulate, known as the relaxation time, and thus as frequency increases this effect may become more and more important and exaggerated and may affect the device's response. A good model for this effect and how it is affected by frequency is presented in [28] and its effects would likely be interesting in a MOSHEMT with multiple gate oxides.

In conclusion, there is still a great deal of work and improvement to be done to perfect the GaN based HEMT. This thesis has suggested specific design choices to move towards a normally off MOSHEMT. Combined with other design and fabrication techniques, a normally off transistor certainly seems attainable. Such a

transistor will be invaluable in the world of modern electronics for creating small, efficient, fast, and high power electronic devices.

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Vita

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